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(54) Liquid crystal display panel with reduced pixel defects.

(57) A liquid crystal display panel has a glass substrate (51), a plurality of rows of gate electrodes (52) provided on the glass substrate, a plurality of columns of drain electrodes (56), a plurality of pixel electrodes (60) corresponding to each of the intersections of a matrix formed by the gate electrodes and the drain electrodes, and first and second insulating films (53,58) between the gate electrodes, the drain electrodes, and the pixel electrodes in order to isolate them from each other. The pixel electrodes (60) communicate with the source electrodes (57) through openings (59) in the second insulating films (58).

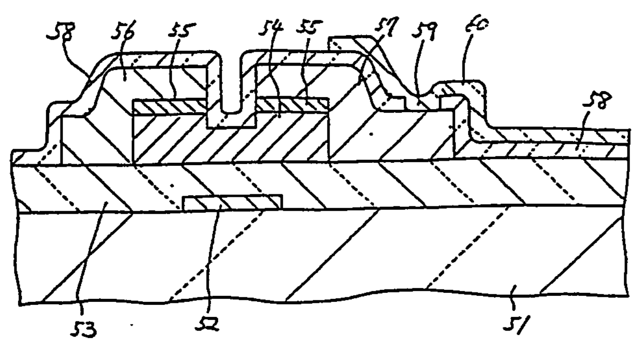

Fig. 5

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LIQUID CRYSTAL DISPLAY PANEL WITH REDUCED PIXEL DEFECTS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a liquid crystal display panel, and more particularly to a liquid crystal display panel with reduced pixel defects.

Description of the Related Art

In recent years, research and development has been pursued actively on liquid crystal displays which make it possible to reduce the thickness of the display panel. In particular, the active matrix addressing method using thin film transistors has been the object of research in view of its potential as a method which is capable of preventing the occurrence of the contrast deterioration problem in liquid crystal display's and enables the creation of a display with a large number of scanning lines (namely, a large capacity).

In applying thin film transistors to a liquid crystal display, it becomes necessary to form a thin film transistor array with satisfactory yield at low cost. In so doing, it is desirable to give the simplest possible structure to the thin film transistor.

As the thin film semiconductor material for the thin film transistor, use is usually made of amorphous silicon, polycrystalline silicon, cadmium sulfide or the like. In FIG. 1 is shown a sectional view of a thin film display as disclosed in Applied Physics, Vol. 24, pp. 357-362, 1981 for the case of using amorphous silicon as the thin film semiconductor material. In this structure, both a gate electrode 21 and a pixel electrode 23 are formed into an island pattern on the same glass substrate 20. This thin film transistor (TFT) element has a gate insulating film 30 formed so as to cover both the gate electrode 21 and the pixel electrode 23, an islandlike semiconductor film 25, a source electrode 29 electrically connected to the pixel electrode 23, and a drain electrode 28 which serves as a signal line.

Further, another structure used for the liquid crystal display which is disclosed in Society of Information Display (SID), p. 310, 1988 is shown in FIG. 2. The present transistor is constituted of a first and a second insulating films 22 and 24 formed so as to cover a gate electrode 21 provided on a glass substrate 20, a semiconductor film 25 formed into an island pattern on the second insulating film 24, and source and drain electrodes 29 and 28 that are electrically connected respectively to source and drain regions 27 formed on the semiconductor film 25. A pixel electrode 23 is formed on the second insulating film 24 to be connected with the source electrode 29. Reference numeral 26 is a protective film.

In the transistor structures shown above, the structure shown in FIG. 1, for example, is designed so as to avoid bringing the gate electrode 21 and the pixel electrode 23 into electrical contact on the glass substrate 20. Further, the structure shown in FIG. 2 is designed so as to avoid the electrical contact between the drain electrode 28 and the pixel electrode 23 in the same plane, as is indicated in the explanatory diagram shown in FIG. 3. However, in the manufacturing process of the transistor array, electrical contact tends to be formed between the gate electrode 21 and the pixel electrode 23 or between the drain electrode 28 and the pixel electrode 23, because of dust that strays into the device during the photoresist process or the like. When such a contact takes place, it is represented as a point defect in the picture display, which becomes a cause for the deterioration in the yield.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a liquid crystal display panel which is capable of reducing the defects in the picture display and producing a high yield with a simple construction.

The liquid crystal display panel according to the present invention includes a substrate and a plurality of pixel elements formed on the substrate in a matrix form, each of the pixel elements having a gate electrode formed on the substrate, a first insulating film provided covering the gate electrode, a pixel electrode provided on or above the first insulating film, a semiconductor layer provided on or above the first insulating film directly above the gate electrode, source and drain regions formed in the semiconductor layer on both sides of the gate electrode, a first electrode connected to one of the source region and the drain region, a second insulating film provided between the pixel electrode and the semiconductor layer, a hole provided in the second insulating film, and a second electrode that connects the pixel element and the other of the source and the drain regions via the hole.

The first electrode that is connected to one of

the source and drain regions, the gate electrode, and the pixel electrode are mutually insulated by means of the first and the second insulating films. Therefore, even when the gate electrode or the first electrode protrudes over the pixel electrode due to dust or the like, which entered into the device during the photoresist process, it will not lead to a picture defect because these electrodes are isolated by the first and the second insulating films. In addition, the structure of the device according to the present invention is such that the increase in the number of fabrication steps over that of the conventional structure is only slight. Therefore, it becomes possible to obtain a thin film transistor array with low cost and high yield.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and further objects, features and advantages of the present invention will become more apparent from the following detailed description taken in conjunction with the accompanying drawings, wherein:

FIGS. 1 and 2 are sectional views of the thin film transistors of the prior art;

FIG. 3 is a plan view for explaining the liquid crystal display panels of the prior art and the present invention;

FIG. 4 is a sectional view for explaining a first embodiment of the present invention;

FIG. 5 is a sectional view for explaining a second embodiment of the present invention; and

FIG. 6 is a sectional view for explaining a third embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

Referring to FIG. 3 again, a plurality of rows of gate electrodes 21 and a plurality of columns of drain electrodes 29 are formed. A plurality of pixel electrodes 23 are formed corresponding to each intersection of a matrix formed by the gate electrodes 21 and the drain electrodes 29.

Referring to FIG. 4, first, chromium is deposited to a thickness of 100 nm on a glass substrate 10, and a gate electrode 11 is formed by patterning the film into island form. Subsequently, after forming a 150 nm thick SiO_x film as a first insulating film 12, indium tin oxide is formed to a thickness of 100 nm which is patterned into island form to create a pixel electrode 13. Then, 300 nm of SiN_x as a second insulating film 14, 100 nm of amorphous silicon as a semiconductor layer 15, and 100 nm of SiN_x as a protective film 16 are formed sequentially by a plasma CVD method at a temperature of about 250°C. Further, after patterning the protective film 16 into island form, an n^+-type amorphous silicon layer doped with an impurity such as phosphorus which serves as a source and drain region 17 is formed to a thickness of 40 nm, and the layer is patterned to avoid electrical contract between the source region and the drain region. Then, after patterning the amorphous silicon layer into island form, a contact hole is opened at a part in the second insulating film 14 over the pixel electrode 13. The contact hole is created by a dry etching using CF_4. Thereafter, chromium is formed to a thickness of 200 nm as the metal for source and drain electrodes, and patterned so as to establish an electrical contact between the pixel electrode 13 and a source electrode 19 via the contact hole and to ensure the electrical isolation between the source electrode 19 and a drain electrode 18, completing the fabrication of the thin film transistor. Then, an upper glass substrate 40 having a transparent electrode 41 thereon is formed above the glass substrate 10. A liquid crystal 42 is inserted between the pixel electrode 13 and the transparent electrode 41.

It should be pointed out that although the first insulating film 12 was formed covering the entire surface in the present embodiment, the film may be formed limited only to the vicinity of the gate electrode as shown in FIG. 2. In that event, the pixel electrode will be formed on the glass substrate.

In the thin film transistor of the present embodiment, a structure is employed in which the protective film 16 is formed directly above the channel section that is formed in the amorphous silicon layer 15 directly above the gate electrode 11. However, the present invention also operates effectively in a structure where the protective film 16 is missing. In that case, the fabrication process differs slightly from that of the present embodiment, requiring the etching of the n^+-type amorphous silicon layer. Moreover, although amorphous silicon is used as the thin film semiconductor in the thin film transistor of the present embodiment, the present invention will also remain effective even when other semiconductors such as polycrystalline silicon and cadmium sulfide are employed.

In the present embodiment, the pixel electrode 13, the drain electrode 18 and the gate electrode 11 are isolated from one another by the insulating films 12 and 14, so that the number of pixel defects due to short-circuiting between these electrodes are reduced, yet the structure is simple. The

number of occurrences of point defects was evaluated by actually forming a liquid crystal display having a thin film transistor array of the present embodiment and carrying out a picture display. The result of the evaluation showed that in contrast to an average number of defect occurrences of 5 per 100 cm^2 in the prior structure, it was improved to an average value of 0.2 in the liquid crystal display using the transistor array of the present structure, confirming that the effect of the present invention is conspicuous.

(Second Embodiment)

FIG. 5 is a schematic vertical sectional view showing important parts of a second embodiment of the present invention, by taking out one unit of thin film transistor.

In a liquid crystal display panel equipped with a plurality of thin film transistor films arranged in array form and a plurality of pixel electrode 60 that are connected respectively to the thin film transistors, the present embodiment has a silicon nitride (SiN_x) film 58 provided as an interlayer insulating film on a source electrode 57 and a drain electrode 56 of the thin film transistor, and the source electrode 57 and the pixel electrode 60 are connected via an opening section 59 provided in the silicon nitride film 58.

In addition, in FIG. 5, 51 is a glass substrate, 52 is a gate electrode, 53 is an insulating film, 54 is an i-a-Si (intrinsic amorphous silicon) layer, and 55 is an n^+-a-Si (n^+-amorphous silicon) layer. An upper glass substrate, a transparent electrode on the upper glass substrate, and a liquid crystal, though they are not shown, are also formed as described in the first embodiment.

One of the features of the present embodiment resides in the provision of the silicon nitride film 58 having an opening section 59.

The method of fabrication of the present embodiment will be described next.

The gate electrode 52 is formed on the glass substrate 51, and 3000 Å of silicon nitride film 53 as a gate insulating film, 3000 Å of the i-a-Si layer 54 as a transistor layer, and 500 Å of the n^+-a-Si layer 55 as an ohmic contact layer are formed respectively. Next, the i-a-Si layer 54 and the n^+-a-Si layer 55 are removed except for the transistor part, and 3000 Å of chromium which is to become the drain electrode 56 and the source electrode 57 is formed by sputtering and then patterned. Then, 1000 Å of silicon nitride film 58 is formed as the interlayer insulating film, an opening section 59 is formed by etching, and 800 Å of ITO (indium tin oxide) film is formed by sputtering, and then patterned into a pixel electrode 60.

According to the present embodiment the silicon nitride film 58 exists between the drain electrode 56 and the pixel electrode 60, and an electrical short-circuiting between these electrodes will not occur even when there exists a defect in photolithography.

(Third Embodiment)

FIG. 6 is a schematic vertical section view showing important parts of a third embodiment of the present invention.

In the present embodiment, the interlayer insulating film is formed with a polyimide film 61, and the source electrode 57 and the pixel electrode 60 are connected via the opening section 59.

One of the features of the present embodiment resides in the fact that the polyimide film 61 with the opening section 59 is provided.

The present embodiment can be fabricated in the same manner as in the second embodiment by forming the polyimide film 61 in place of the silicon nitride film 58.

The present embodiment has an advantage that the surface of the thin film transistor array can be made flat so that the gap control and the orientation control in the formation of the liquid crystal panel are facilitated.

It should be noted that although the description has been given above is based on the connection formed between the pixel electrode and the source electrode as an example, similar effect can be realized for the case of connecting the pixel electrode and the drain electrode.

Claims

1. A liquid crystal display panel comprising:
a substrate; and
a plurality of pixel elements formed on said substrate in a matrix form, each of said pixel elements having
a gate electrode provided on said substrate,
a first insulating film provided covering said gate electrode,
a pixel electrode provided on or above said first insulating film,
a semiconductor layer provided on or above said first insulating film directly above said gate electrode,
a source region and a drain region formed in said semiconductor layer on both sides of said gate electrode,
a first electrode connected to one of said source region or said drain region,
a second insulating film provided between said

pixel electrode and said semiconductor layer, a hole provided in said second insulating film, and a second electrode connecting the other of said source region or said drain region and said pixel electrode through said hole.

2. A liquid crystal display panel as claimed in claim 1, wherein said second insulating film is provided on said semiconductor layer and said first electrode, and said pixel electrode is provided on said second insulating film.

3. A liquid crystal display panel as claimed in claim 1, wherein said second insulating film is provided on said pixel electrode, and said semiconductor layer and said first electrode are provided on said second insulating film.

4. A liquid crystal display panel as claimed in claim 1, wherein said substrate is a glass substrate, said first insulating film is a silicon oxide or a silicon nitride film, said semiconductor layer is an amorphous silicon layer, and said second insulating film is a silicon nitride film.

5. A liquid crystal display panel as claimed in claim 1, wherein said substrate is a glass substrate, said semiconductor layer is an amorphous silicon layer, and said second insulating film is a polyimide film.

6. A liquid crystal display panel comprising:
a substrate;
a plurality of rows of gate electrode provided on said substrate;
a plurality of columns of one of source electrode and drain electrode provided above said substrate;
a plurality of pixel electrodes provided above said substrate corresponding to each intersection of a matrix formed by said plurality of rows of gate electrode and said plurality of columns of said one of source electrode and drain electrode;
a first insulating film provided between said plurality of rows of gate electrode and said plurality of columns of said one of said source electrode and said drain electrode;
a second insulating film provided between said plurality of pixel electrodes and said plurality columns of said one of said source electrode and said drain electrode;
holes provided in said second insulating film; and
a plurality of semiconductor layers provided on said first insulating film directly above said plurality of rows of gate electrode,each of said plurality of semiconductor layers having a source region and a drain region on the respective sides of said gate electrode, said plurality of semiconductor layers being respectively connected to said pixel electrodes, by connecting one of said source region and said drain region to the corresponding one of said source electrode or said drain electrode and by connecting the other of said source region and said drain region to said pixel electrode via sia hole, respectively.

7. A liquid crystal display panel as claimed in claim 6, wherein said substrate is a glass substrate, said first and second insulating films are silicon nitride films, and said semiconductor layer is an amorphous silicon layer.

8. A liquid crystal display panel as claimed in claim 6, wherein said substrate is a glass substrate, said first insulating film is a silicon nitride film, said second insulating film is a polyimide film, and said semiconductor layer is an amorphous silicon layer.

9. A liquid crystal display panel comprising:
a substrate;
a plurality of rows of gate electrode provided on said substrate;
a plurality of columns of one of source electrode and drain electrode provided above said substrate;
a plurality of pixel electrodes provided above said substrate corresponding respectively to each of the intersections of a matrix formed by said plurality of rows of gate electrode and said plurality of columns of said one of source electrode and drain electrode;
a first insulating film provided between said plurality of rows of gate electrode and said plurality of pixel electrodes;
a second insulating film provided between said plurality of pixel electrodes and said plurality of columns of said one of said source electrode or said drain electrode;
holes provided in said second insulating film; and
a plurality of semiconductor layers provided on said second insulating film directly above said plurality of rows of gate electrode, each of said plurality of semiconductor layers having a source region and a drain region on the respective sides of said gate electrode, said plurality of semiconductor layers being respectively connected to said pixel electrodes by connecting one of said source region or said drain region to the corresponding one of said source electrode or said drain electrode and by connecting the other of said source region and said drain region to said pixel electrode via said hole, respectively.

10. A liquid crystal display panel as claimed in claim 9, wherein said substrate is a glass substrate, said first insulating film is a silicon oxide, said second insulating film is a silicon nitride, and said semiconductor layer is an amorphous silicon layer.

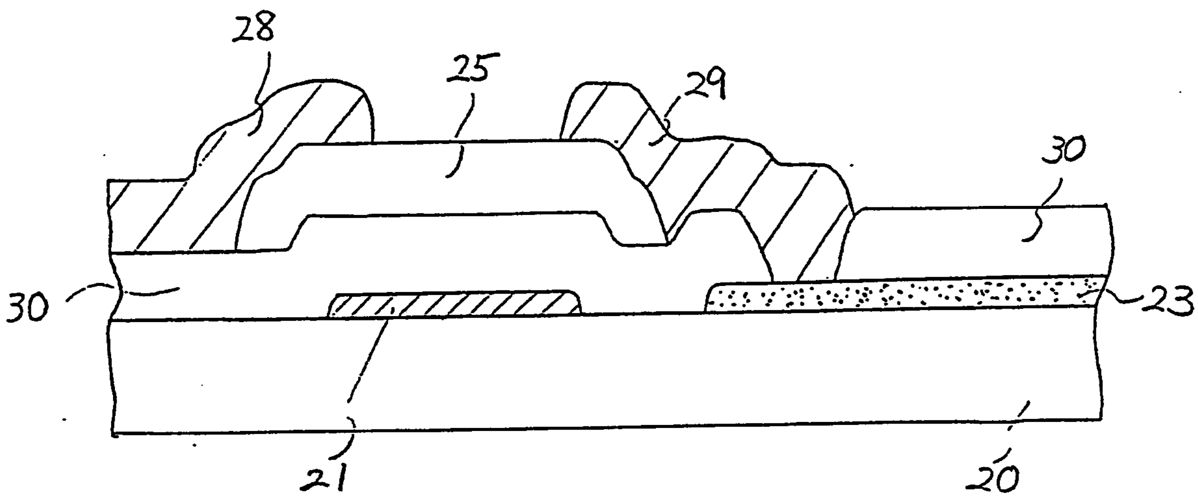

Fig. 1 (PRIOR ART)

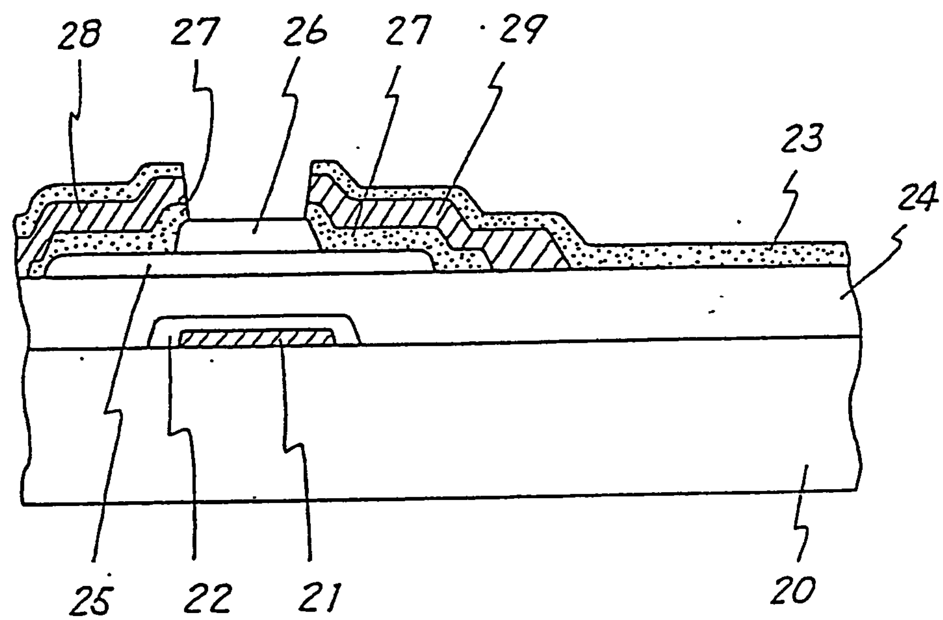

Fig. 2 (PRIOR ART)

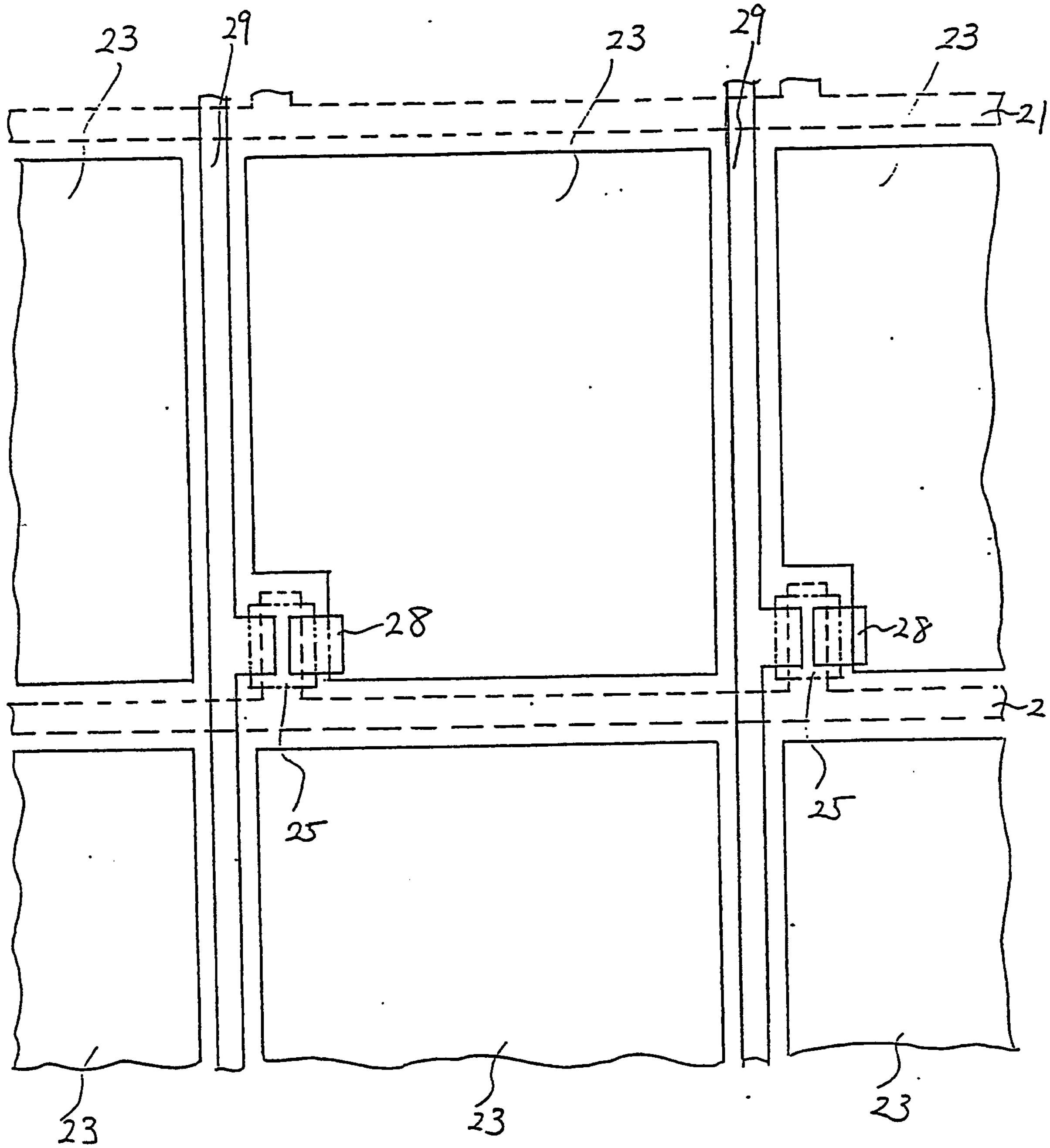

Fig. 3

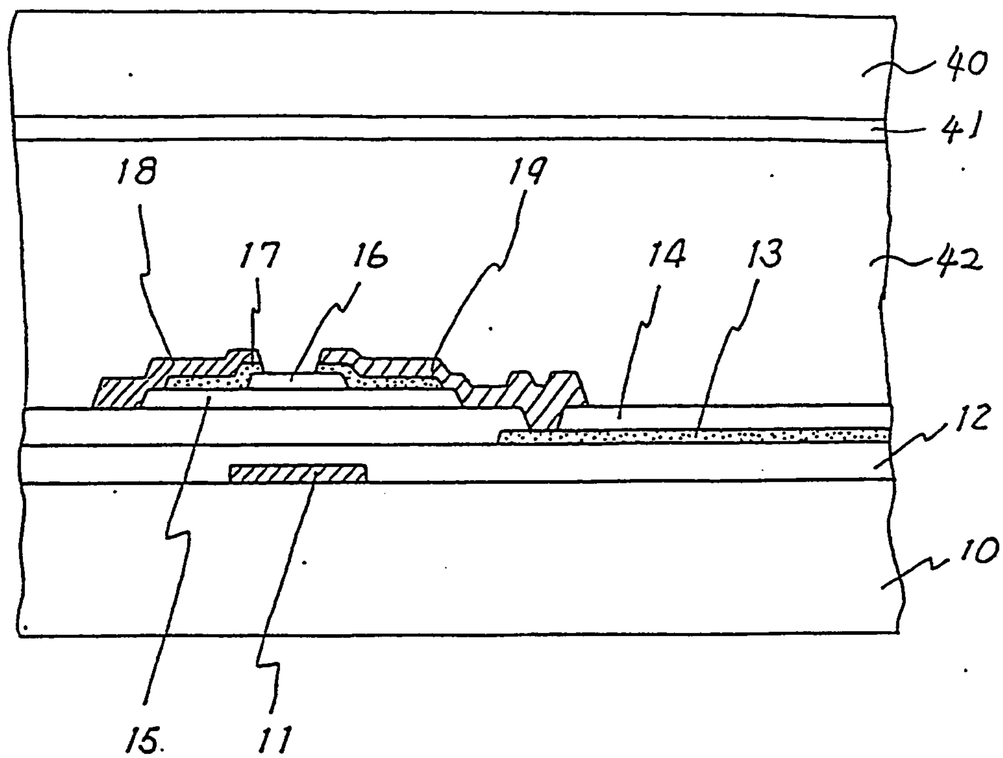

Fig. 4

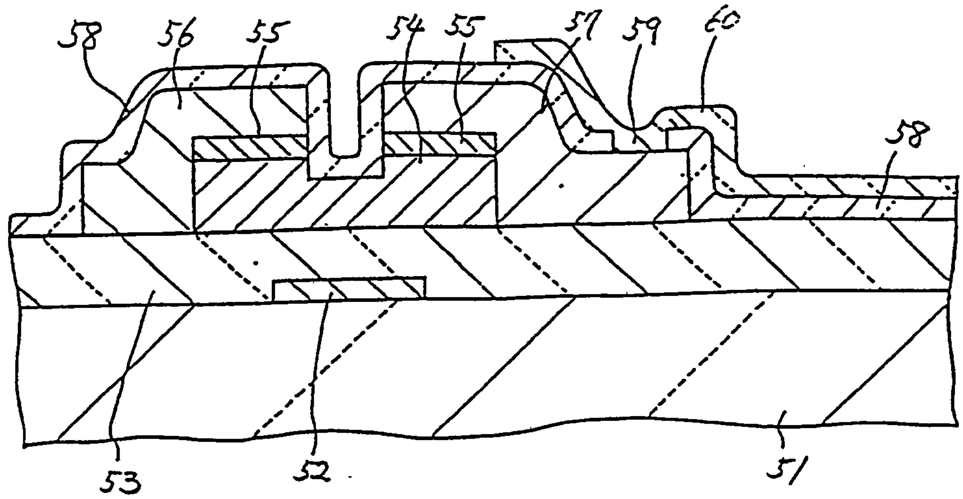

Fig. 5

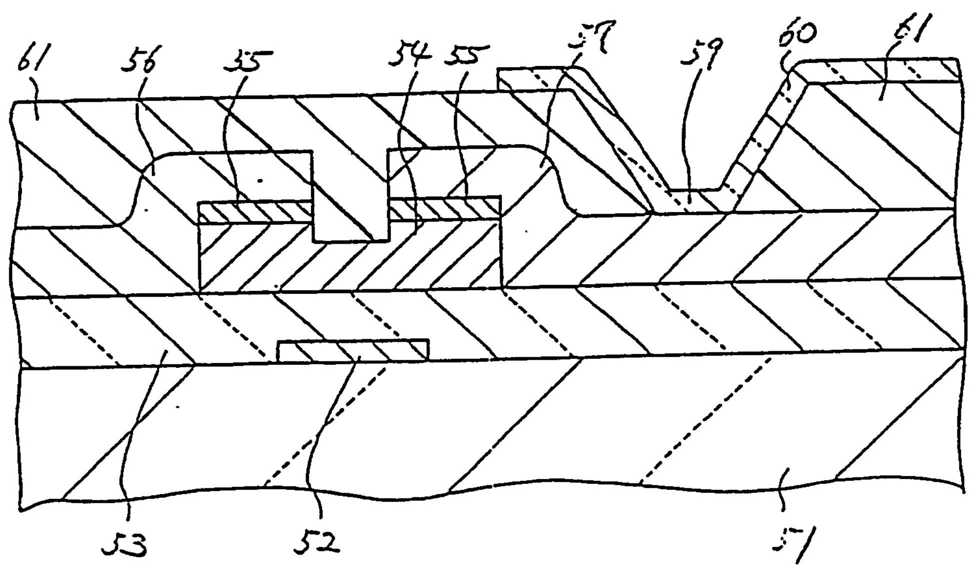

Fig. 6